CLAIM AMENDMENTS

1. (currently amended) For a communication system wherein a transmitted ~~signal (VX)~~ signal is distorted to become a received ~~signal (VR)~~ signal, wherein the transmitted signal comprises a sequence of data cycles of uniform duration, wherein during a portion of some data cycles the transmitted signal is of substantially constant high magnitude and during a portion of all every other data ~~cycle~~ cycles the transmitted signal is of substantially constant low magnitude, such that a pattern of high and low magnitudes represents a sequence of symbols, a method for processing the received signal to produce a first data ~~signal (Z)~~ signal representing the sequence of symbols, the method comprising the steps of:

filtering the received signal with a transfer function controlled by at least one filter control signal to produce a compensated ~~signal (X)~~ signal;

processing the compensated signal to generate a sampling clock ~~signal (CLK)~~ signal having a plurality of successive cycles of said uniform duration wherein a leading edge of the sampling clock signal occurs at a start of each sampling clock signal cycle and a trailing edge of the sampling clock signal occurs substantially at a middle of each sampling clock signal cycle;

generating the first data signal having successive states representing magnitudes of the compensated signal on successive leading edges of the sampling clock signal;

generating a second data signal having successive states representing magnitudes of the compensated signal on successive trailing edges of the sampling clock signal; and

generating the at least one filter control signal as a function of the first and second data signals.

2. (original) The method in accordance with claim 1 wherein the step of filtering the received signal comprises attenuating low frequency components of the received signal by an amount that is a function of the at least one filter control signal to produce the compensated signal.

3. (original) The method in accordance with claim 1 wherein the step of filtering the received signal comprises amplifying high frequency components of the received signal by an amount that is a function of the at least one filter control signal to produce the compensated signal.

4. (currently amended)The method in accordance with claim 1 wherein the step of filtering the received signal comprises the substeps of:

generating an offset ~~signal (A)~~ signal as a function of the received signal and of the at least one filter control signal; and

subtracting the offset signal from the received signal to produce the compensated signal.

5. (currently amended) The method in accordance with claim 1 wherein the step of filtering the received signal comprises the substeps of:

generating an offset ~~signal (A)~~ signal as a function of the received signal and of the at least one filter control signal; and

adding the offset signal to the received signal to produce the compensated signal.

6. (currently amended) The method in accordance with claim 1 wherein the step of filtering the received signal comprises the substeps of:

generating an offset ~~signal (F)~~ signal as a function of the first data signal and of the at least one filter control signal, and

subtracting the offset signal from the received signal to produce the compensated signal.

7. (currently amended)The method in accordance with claim 6 wherein at least one filter control signal comprises first and second control signals ~~are~~ generated as the following functions of the first and second data signals:

$G1_{n+1} = G1_n + \Delta_+$ when $S_{n-1} = Z_{n-2}$, else $G1_{n+1} = G1_n - \Delta_-$

$G2_{n+1} = G2_n + \Delta_+$ when $S_{n-1} = Z_{n-3}$, else $G2_{n+1} = G2_n - \Delta_-$

wherein

$G1_n$ is a magnitude of the first filter control signal during an n^{th} sampling clock signal cycle,

$G1_{n+1}$ is a magnitude of the first filter control signal during an $(n+1)^{th}$ sampling clock signal cycle,

$G2_n$ is a magnitude of the second filter control signal during the n^{th} sampling clock signal cycle,

$G2_{n+1}$ is a magnitude of the second filter control signal during the $(n+1)^{th}$ sampling clock signal cycle,

Z_{n-2} is a state of the first data signal following an $(n-2)^{th}$ trailing edge of the sampling clock signal

Z_{n-3} is a state of the first data signal following an $(n-3)^{th}$ trailing edge of the sampling clock signal,

S_{n-1} is a state of the second data signal following an $(n-1)^{th}$ trailing edge of the sampling clock signal, and

Δ_+ and Δ_- ~~Δ_+ and Δ_-~~ are constants.

8. (currently amended) The method in accordance with claim 7 wherein during each nth sampling clock cycle the offset signal is of magnitude ~~$G1_n{*}Z_{n+1} + G2_n{*}Z_n$ wherein Z_n~~ $G1_n{*}Z_{n-1} \pm G2_n{*}Z_{n-1}$, wherein Z_{n-1} is a state of the first data signal following each n^{th} trailing edge of the sampling clock signal.

9. (currently amended) The method in accordance with claim 1 ~~wherein one filter control signal~~ the at least one filter control signal is generated as the following function of the first and second data signals:

$G_{n+1} = G_n$, when $Z_n = Z_{n-1}$,

$G_{n+1} = G_n + \Delta_+$ when $S_{n-1} = Z_{n-2}$, else

$G_{n+1} = G_n - \Delta_-$

wherein

G_n is a magnitude of the one filter control signal during an n^{th} sampling clock signal cycle,

G_{n+1} is a magnitude of the one filter control signal during an $(n+1)^{th}$ sampling clock signal,

Z_n is a state of the first data signal following an n^{th} trailing edge of the sampling clock signal,

Z_{n-1} is a state of the first data signal following an $(n-1)^{th}$ trailing edge of the sampling clock signal,

Z_{n-2} is a state of the first data signal following an $(n-2)^{th}$ trailing edge of the sampling clock signal,

S_{n-1} is a state of the second data signal following the $(n-1)^{th}$ trailing edge of the sampling clock signal, and

Δ_+ and Δ_- are constants.

10. (currently amended) The method in accordance with claim 1 wherein the step of generating the first data signal comprises the substeps of:

sampling the compensated signal on each leading edge of the compensated signal to produce a sample ~~signal (Y), the second~~ signal and the second data signal; and

sampling the sample signal on each trailing edge of the compensated signal to produce the first data signal.

11. (original) The method in accordance with claim 1 wherein the step of generating a second data signal comprises sampling the compensated signal on each trailing edge of the compensated signal to produce the second data signal.

12. (original) The method in accordance with claim 1

wherein the step of generating the first data signal comprises responding to trailing edges of the sampling clock signal by driving the first data signal to a succession of first states, wherein each first state corresponds to a separate leading edge of the sampling clock signal and represents a magnitude of the compensated signal on occurrence of the first state's corresponding sampling clock signal leading edge, and

wherein the step of generating a second data signal comprises responding to trailing edges of the sampling clock signal by generating a second data signal by driving the second data signal to a succession of second states, wherein each second state corresponds to a separate trailing edge of the sampling clock signal and represents a magnitude of the compensated signal on occurrence of the second state's corresponding sampling clock trailing edge.

13. (currently amended) For a communication system wherein a transmitted ~~signal (VX)~~ signal is distorted to become a received ~~signal (VR)~~ signal, wherein the transmitted signal comprises a sequence of data cycles of uniform duration representing a sequence of transmitted symbols, wherein during a middle portion of some data cycles the transmitted signal is of substantially constant high magnitude and during a middle portion of all other data cycles the transmitted signal is of substantially constant low magnitude, an apparatus for processing the received signal to produce a first data ~~signal (Z)~~ signal representing the sequence of transmitted symbols, the apparatus comprising:

a first circuit for filtering the received signal with a transfer function controlled by at least one filter control signal to produce a compensated ~~signal (X)~~ signal;

a second circuit for processing the compensated signal to generate a sampling clock ~~signal (CLK)~~ signal having a plurality of successive cycles of substantially uniform duration wherein a leading edge of the sampling clock signal occurs at a start of each sampling clock signal cycle and a trailing edge of the sampling clock signal occurs substantially at a middle of each sampling clock signal cycle;

a third circuit for generating the first data signal and a second data signal, wherein successive states of the first data signal represent sampled magnitudes of the compensated signal on successive leading edges of the sampling clock signal, wherein successive states of the second data signal represent sampled magnitudes of the compensated signal on successive trailing edges of the sampling clock signal; and

a fourth circuit for generating the at least one filter control signal as a function of the first and second data signals.

14. (original) The apparatus in accordance with claim 13 wherein the first circuit comprises attenuating low frequency components of the received signal by an amount that is a function of the at least one filter control signal to produce the compensated signal.

15. (original) The apparatus in accordance with claim 13 wherein the first circuit amplifies high frequency components of the received signal by an amount that is a function of the at least one filter control signal to produce the compensated signal.

16. (currently amended)The apparatus in accordance with claim 13 wherein the first circuit generates an offset ~~signal (A)~~ signal as a function of the received signal and of the at least one filter control signal, and subtracts the offset signal from the received signal to produce the compensated signal.

17. (currently amended) The apparatus in accordance with claim 13 wherein the first circuit generates an offset ~~signal (A)~~ signal as a function of the received signal and of the at least one filter control signal and adds the offset signal to the received signal to produce the compensated signal.

18. (currently amended)The apparatus in accordance with claim 13 wherein the first circuit generates an offset ~~signal (F)~~ signal as a function of the first data signal and of the at least one filter control signal, and subtracts the offset signal from the received signal to produce the compensated signal.

19. (currently amended) The apparatus in accordance with claim 18 wherein the fourth circuit ~~generates the~~ generates the at least one filter control signal comprising first and second control ~~signals a~~ signals as the following functions of the first and second data signals:

$G1_{n+1} = G1_n + \Delta$ when $S_{n-1} = Z_{n-2}$, else $G1_{n+1} = G1_n - \Delta_-$

$G2_{n+1} = G2_n + \Delta_+$ when $S_{n-1} = Z_{n-3}$, else $G2_{n+1} = G2_n - \Delta_-$

wherein

$G1_n$ is a magnitude of the first filter control signal during an n^{th} sampling clock signal cycle,

$G1_{n+1}$ is a magnitude of the first filter control signal during an $(n+1)^{th}$ sampling clock signal cycle,

$G2_n$ is a magnitude of the second filter control signal during the n^{th} sampling clock signal cycle,

$G2_{n+1}$ is a magnitude of the second filter control signal during the $(n+1)^{th}$ sampling clock signal cycle,

Z_{n-2} is a state of the first data signal following an $(n-2)^{th}$ trailing edge of the sampling clock signal

Z_{n-3} is a state of the first data signal following an $(n-3)^{th}$ trailing edge of the sampling clock signal,

S_{n-1} is a state of the second data signal following an $(n-1)^{th}$ trailing edge of the sampling clock signal, and

Δ_+ and Δ_- ~~Δ and Δ~~ are constants.

20. (currently amended) The apparatus in accordance with claim 19 wherein during each nth sampling clock cycle the offset signal is of magnitude ~~$G1_n{*}Z_{n-1} + G2_n{*}Z_n$ wherein Z_n~~ $G1_n{*}Z_n + G2_n{*}Z_{n-1}$. wherein Z_{n-1} is a state of the first data signal following each n^{th} trailing edge of the sampling clock signal.

21. (currently amended) The apparatus in accordance with claim 13 wherein the fourth circuit generates ~~one filter control signal~~ the at least one filter control signal as the following function of the first and second data signals:

$G_{n+1} = G_n$, when $Z_n = Z_{n-1}$,

$G_{n+1} = G_n + \Delta$ when $S_{n-1} = Z_{n-2}$, else

$G_{n+1} = G_n - \Delta_-$

wherein

G_n is a magnitude of the one filter control signal during an n^{th} sampling clock signal cycle,

G_{n+1} is a magnitude of the one filter control signal during an $(n+1)^{th}$ sampling clock signal,

Z_n is a state of the first data signal following an n^{th} trailing edge of the sampling clock signal,

Z_{n-1} is a state of the first data signal following an $(n-1)^{th}$ trailing edge of the sampling clock signal,

Z_{n-2} is a state of the first data signal following an $(n-2)^{th}$ trailing edge of the sampling clock signal,

S_{n-1} is a state of the second data signal following the $(n-1)^{th}$ trailing edge of the sampling clock signal, and

Δ_+ and Δ_- ~~Δ and Δ~~ are constants.

22. (currently amended) The apparatus in accordance with claim 13 wherein the third circuit samples the compensated signal on each leading edge of the compensated signal to produce a sample signal ~~(Y), the second data signal, and samples~~ and the second data signal, and samples the sample signal on each trailing edge of the compensated signal to produce the first data signal.

23. (original) The apparatus in accordance with claim 13 wherein the third circuit samples the compensated signal on each trailing edge of the compensated signal to produce the second data signal.

24. (original) The apparatus in accordance with claim 13

wherein the third circuit responds to trailing edges of the sampling clock signal by driving the first data signal to a succession of first states, wherein each first state corresponds to a separate leading edge of the sampling clock signal and represents a magnitude of the compensated signal on occurrence of the first state's corresponding sampling clock signal leading edge, and

wherein the third circuit responds to trailing edges of the sampling clock signal by generating a second data signal by driving the second data signal to a succession of second states, wherein each second state corresponds to a separate trailing edge of the sampling clock signal and represents a magnitude of the compensated signal on occurrence of the second state's corresponding sampling clock trailing edge.